ABSTRACT OF THE DISCLOSURE

A BIST circuit for an IC measures the time delay a rising or falling edge experiences as it passes through a signal path within the IC. A strobe circuit within the BIST circuit generates edges in two signals A and B in delayed response to edges of a STROBE signal. A path probe generates a signal C edge at the signal path input in response to each signal A edge. The STROBE-to-B edge delay within the strobe generator is iteratively adjusted to determine a first delay for which the path probe detects the B and C signal edges at nearly the same time and thereafter iteratively adjusted to determine a second delay for which the path probe detects the B and D signal edges at nearly the same time. The first delay is measured by causing the strobe signal generator to produce a periodic signal having a period proportional to the first delay and counting the number of cycles of a reference clock occurring during K cycles of the periodic signal. The second delay is measured in a similar manner. The path delay is determined as a difference between the measured first and second delays.